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EXAMINER	
CHUNG, HOON J	

ART UNIT	PAPER NUMBER
2416	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/582,150	HIPP, IMRE	
	Examiner	Art Unit	
	HOON J. CHUNG	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *June 08, 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) *1-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *June 08, 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *June 08, 2006 and August 30, 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Please note that AU 2616 has been changed to AU 2416.

2. Claims 1-22 are withdrawn.

3. Claims 23-41 are added.

Priority

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 10357477.8, filed on December 09, 2003.

Information Disclosure Statement

5. The information disclosure statement (IDS) submitted on June 08, 2006 and August 30, 2006 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

6. Claims 33-40 are objected to because of the following informalities: the phrase "where in the first network unit a bus signal **being** formed from at least one channel signal" in lines 4-5 of claim 33 should be changed to "**,** where in the first network unit a bus signal **is** formed from at least one channel signal". Appropriate correction is required.

7. Claim 41 is objected to because of the following informalities: the phrase "**a bus signal created a plurality** of channel signals" in line 9 of claim 41 should be changed to "a bus signal **is** created **from** a plurality of channel signals". Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 27-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 27, it is not clear what the phrase "**below the encoding units**" in line 5 means. The claim does not introduce any hierarchy in regard to different units.

For the purpose of examination, the phrase "**below the encoding units**" is considered as "**outside the encoding units**". Furthermore, since there is no distinction made with regard to pulse width information, the non-encoding units may or may not process pulse width information.

10. Claims 37-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 37, it is not clear what the phrase "**below the encoding units**" in line 2 means. The claim does not introduce any hierarchy in regard to different units. For the purpose of examination, the phrase "**below the encoding units**" is considered as "**outside the encoding units**". Furthermore, since pulse width information is not considered outside the encoding units, what non-encoding units perform with regard to pulse width information is not pertaining to the invention.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (US Patent No. 5,673,004, hereinafter Park '004) in view of Hogeboom (US Patent No. 6,262,998 B1, hereinafter Hogeboom '998).

Regarding claim 23, Park '004 discloses a circuit for clock synchronization between a first network unit (figure 3 of Park '004) and a second network unit (it is implied that there is a second network unit, since clock synchronization is done between a plurality of network units), comprising:

a clock recovery unit (unit 22 in figure 3 of Park '004) having at least one reference clock signal provided in the first network unit (reference timing signals A and B are provided to the unit 22 in figure 3 of Park '004);

a bus provisioning unit (CPU 24 in figure 3 of Park '004) with an encoding unit (unit 23 in figure 3 of Park '004) arranged in the first network unit where the encoding unit is used for creating a channel signal (Fsys1 signal in figure 3 of Park '004) from the reference clock signal (column 4, lines 49-55 of Park '004 disclose generating a system clock Fsys1 using a reference clock).

However, Park '004 does not explicitly disclose a bus signal being created from a plurality of channel signals and forwarded to a decoder unit in the second network unit.

Hogeboom '998 discloses a bus signal being created from a plurality of channel signals (column 4, lines 48-53 and figure 4 of Hogeboom '998 discloses a data bus channel 404 and a control information/clock bus channel 406) and

forwarded to a decoder unit in the second network unit (figure 4 of Hogeboom '998 discloses decoding unit 402 receiving clock, control information and data).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to create a bus signal and forward the bus signal to a second network unit, since the modification, as suggested in column 2, lines 12-15 of Hogeboom '998, provides an efficient means of achieving both a synchronous clock and a control channel integrated in a single signal path used with a high-speed parallel data bus.

Regarding claim 24, Park '004 and Hogeboom '998 disclose the circuit of claim 23, wherein the encoding unit is configured such that a sequence of individual pulses with a defined distance is created from the reference clock signal present on the input side (column 4, lines 49-55 of Park '004 disclose generating a system clock Fsys1 of 51.84 MHz; a frequency has a specific distance/time between each pulse).

Regarding claim 25, Park '004 and Hogeboom '998 disclose the circuit of claim 24, wherein the encoding unit is configured such that the defined distances of the pulses are different for each channel signal (column 4, lines 48-53 and figure 4 of Hogeboom '998 discloses a data bus channel 404 and a control information/clock bus channel 406; data signal and the clock signal generally have different amount of information contained within, therefore it is implied that the signals have different frequency, i.e. defined distances of the pulses are different).

Regarding claim 26, Park '004 and Hogeboom '998 disclose the circuit of claim 25, wherein the encoding unit is configured such that the number of pulses created in each channel signal corresponds to the maximum possible number(s) of the encoding units (figure 4 of Hogeboom '998 discloses that there is one, i.e. an example of

maximum possible number, encoding unit 400; figure 1 of Hogeboom '998 discloses a signal, in which there is a single pulse in a period, i.e. 1 pulse per period for an encoding unit).

Regarding claim 27, Park '004 and Hogeboom '998 disclose the circuit of claim 26, wherein the encoding unit is configured so: the width of the created pulses are different (figure 3 of Hogeboom '998 discloses a pulse with a fixed falling edge and a plurality of rising edges 50, 50', 50" and 50"', in which each rising edge is in a different phase; the pulses comprising the fixed falling edge and each rising edge have different widths),

the width of the pulses (figure 3 of Hogeboom '998 discloses a plurality of phase differentiated pulses) created are embodied in ascending order (neither the claim nor the specification clearly defines what advantage embodying the width of the pulses in ascending order provides; since figure 3 of Hogeboom '998 discloses that pulses of different phase modulation have different widths, the pulse can be created from the lowest width to the highest width, i.e. there is nothing in Hogeboom '998 that would prevent this from happening), and

no distinction is made with regard to pulse width information outside the encoding units (column 4, lines 50-53 of Hogeboom '998 disclose the encoding unit generating clock information and combining the clock information with the control data; since the encoding unit handles generation of combined clock information and control data, i.e. involving pulse width information, it is implied that other units of the first network unit are not involved with pulse width information).

Regarding claim 28, Park '004 and Hogeboom '998 disclose the circuit of claim 27, wherein the bus provision unit is configured so the channel signals are grouped together via a summation unit (figure 4 of Hogeboom '998 disclose the encoding unit 400 grouping data and control information channel signals; column 4, lines 48-53 of Hogeboom '998 disclose the encoding unit grouping control information and clock signal) and

signal amplification unit (figure 3 of Park '004 discloses a voltage controlled oscillator 25; VCO allows control of various characteristics of a signal including amplitude)

into a bus signal (figure 4 of Hogeboom '998 discloses transmitting the signals on a data bus).

13. Claims 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (US Patent No. 5,673,004, hereinafter Park '004) in view of Hogeboom (US Patent No. 6,262,998 B1, hereinafter Hogeboom '998) as applied to claim 23 above, and further in view of Heflin (US Patent No. 5,572,554, hereinafter Heflin '554).

Regarding claim 29, Park '004 and Hogeboom '998 do not explicitly disclose the circuit of claim 23, wherein the decoding unit has a pulse width filter and a pulse distance filter.

Heflin '554 discloses a pulse width filter (column 6, lines 18-20 of Heflin '554 disclose a pulse width filter on a second network unit, i.e. decoder of Hogeboom '998 is on the second network unit) and

a pulse distance filter (column 6, lines 27-29 of Heflin '554 disclose a pulse limiter that limits the duration of a pulse to one clock cycle of the local oscillator clock; if a pulse's width is greater than a clock cycle of the local oscillator clock, then the pulse would overlap with another pulse with respect to the clock cycle of the local oscillator clock; therefore the pulse limiter limits the distance between two pulses to 0 or greater with respect to the clock cycle of the local oscillator clock).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a pulse width filter and a pulse distance filter, since the modification, as suggested in column 6, lines 20-22 of Heflin '554, prevents noise spikes from driving the synchronization circuit.

Regarding claim 30, Park '004, Hogeboom '998 and Heflin '554 disclose the circuit of claim 29, wherein the decoding unit is configured so that decoding is performed by a mask function, where the received bus signal is not sampled (column 6, lines 18-20 of Heflin '554 disclose not passing pulses that are shorter than a threshold, i.e. the decoding unit of Hogeboom '998 does not receive the pulses) and

the selection occurs by masking out the non required pulses (i.e. the decoding unit of Hogeboom '998 only receives pulses that are longer than or equal to a threshold).

Regarding claim 31, Park '004, Hogeboom '998 and Heflin '554 disclose the circuit of claim 30, wherein the created pulses having different pulse width and pulse distance are coordinated for simultaneous collision free (i.e. pulse limiter of Heflin '554

prevents two pulses from being overlapped with respect to the clock cycle of the local oscillator clock, therefore the pulses are collision free)

real-time transmission of the clock signals (column 10, lines 22-26 of Heflin '554 disclose that pulse limiter prevents a count sequence of counter/divider from being delayed, i.e. processed without delay or real-time).

Regarding claim 32, Park '004, Hogeboom '998 and Heflin '554 disclose the circuit of claim 31, wherein the selection of an individual channel signal from the bus signal is performed independently by the second network unit (column 4, lines 55-62 and figure 4 of Hogeboom '998 disclose the decoding unit receiving both data channel and control information/clock channel, in which the decoding unit sends data to the data processing device 408, and extracts clock information and control information from a channel based on an signal encoding protocol; since the decoding unit knows the signal encoding protocol, it is implied that the decoding unit can select channel and decode data without any instruction from the encoding unit or the first network unit).

14. Claims 33-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (US Patent No. 5,673,004, hereinafter Park '004) in view of Hogeboom (US Patent No. 6,262,998 B1, hereinafter Hogeboom '998) and Heflin (US Patent No. 5,572,554, hereinafter Heflin '554).

Regarding claim 33, Park '004 discloses a method for clock synchronization between a first network unit (figure 3 of Park '004) and a second network unit (it is

implied that there is a second network unit, since clock synchronization is done between a plurality of network units), comprising:

providing a reference clock signal in the first network unit (reference timing signals A and B are provided to the unit 22 in figure 3 of Park '004) by a clock recovery unit (unit 22 in figure 3 of Park '004); and

forming a channel signal (Fsys1 signal in figure 3 of Park '004) from a reference clock signal (column 4, lines 49-55 of Park '004 disclose generating a system clock Fsys1 using a reference clock).

However, Park '004 does not explicitly disclose a bus signal being formed from at least one channel signal in the first network unit and is forwarded to the second network; and creating pulses having different pulse width and pulse distance.

Hogeboom '998 discloses a bus signal being formed from at least one channel signal in the first network unit (column 4, lines 48-53 and figure 4 of Hogeboom '998 discloses a data bus channel 404 and a control information/clock bus channel 406) and

is forwarded to the second network (figure 4 of Hogeboom '998 discloses decoding unit 402 receiving clock, control information and data); and

creating pulses having different pulse width (figure 3 of Hogeboom '998 discloses a pulse with a fixed falling edge and a plurality of rising edges 50, 50', 50" and 50"', in which each rising edge is in a different phase; the pulses comprising the fixed falling edge and each rising edge have different widths) and

pulse distance (column 4, lines 48-53 and figure 4 of Hogeboom '998 discloses a data bus channel 404 and a control information/clock bus channel 406; data signal and

the clock signal generally have different amount of information contained within, therefore it is implied that the signals have different frequency, i.e. defined distances of the pulses are different for different signals).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to create a bus signal and forward the bus signal to a second network unit, since the modification, as suggested in column 2, lines 12-15 of Hogeboom '998, provides an efficient means of achieving both a synchronous clock and a control channel integrated in a single signal path used with a high-speed parallel data bus.

Furthermore, Park '004 and Hogeboom '998 do not explicitly disclose coordinating pulse distance and pulse width encoding for simultaneous collision free real-time transmission of the clock signals.

Heflin '554 discloses coordinating pulse distance (column 6, lines 27-29 of Heflin '554 disclose a pulse limiter that limits the duration of a pulse to one clock cycle of the local oscillator clock; if a pulse's width is greater than a clock cycle of the local oscillator clock, then the pulse would overlap with another pulse with respect to the clock cycle of the local oscillator clock; therefore the pulse limiter limits the distance between two pulses to 0 or greater with respect to the clock cycle of the local oscillator clock) and

pulse width (column 6, lines 18-20 of Heflin '554 disclose a pulse width filter on a second network unit, i.e. decoder of Hogeboom '998 is on the second network unit) encoding for simultaneous collision free (i.e. pulse limiter of Heflin '554 prevents two

pulses from being overlapped with respect to the clock cycle of the local oscillator clock, therefore the pulses are collision free)

real-time transmission of the clock signals (column 10, lines 22-26 of Heflin '554 disclose that pulse limiter prevents a count sequence of counter/divider from being delayed, i.e. processed without delay or real-time).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a pulse width filter and a pulse distance filter, since the modification, as suggested in column 6, lines 20-22 of Heflin '554, prevents noise spikes from driving the synchronization circuit.

Regarding claim 34, Park '004, Hogeboom '998 and Heflin '554 disclose the method of claim 33, wherein the sequence of individual pulses with a defined distance is created from the reference clock signal present on the input side (column 4, lines 49-55 of Park '004 disclose generating a system clock Fsys1 of 51.84 MHz; a frequency has a specific distance/time between each pulse).

Regarding claim 35, Park '004, Hogeboom '998 and Heflin '554 disclose the method of claim 34, wherein the defined distances of the pulses are characterized differently in each channel signal (column 4, lines 48-53 and figure 4 of Hogeboom '998 discloses a data bus channel 404 and a control information/clock bus channel 406; data signal and the clock signal generally have different amount of information contained within, therefore it is implied that the signals have different frequency, i.e. defined distances of the pulses are different for different signals) and

the number of pulses generated in each channel signal corresponds to a maximum possible number of the encoding units (figure 4 of Hogeboom '998 discloses that there is one, i.e. an example of maximum possible number, encoding unit 400; figure 1 of Hogeboom '998 discloses a signal, in which there is a single pulse in a period, i.e. 1 pulse per period for an encoding unit).

Regarding claim 36, Park '004, Hogeboom '998 and Heflin '554 disclose the method of claim 35, wherein the created pulses are created in ascending order (neither the claim nor the specification clearly defines what advantage embodying the width of the pulses in ascending order provides; since figure 3 of Hogeboom '998 discloses that pulses of different phase modulation have different widths, the pulse can be created from the lowest width to the highest width, i.e. there is nothing in Hogeboom '998 that would prevent this from happening)

relative to their pulse width (figure 3 of Hogeboom '998 discloses a plurality of phase differentiated pulses).

Regarding claim 37, Park '004, Hogeboom '998 and Heflin '554 disclose the method of claim 36, wherein pulse width information is not considered outside the encoding units (column 4, lines 50-53 of Hogeboom '998 disclose the encoding unit generating clock information and combining the clock information with the control data; since the encoding unit handles generation of combined clock information and control data, i.e. involving pulse width information, it is implied that other units of the first network unit are not involved with pulse width information).

Regarding claim 38, Park '004, Hogeboom '998 and Heflin '554 disclose the method of claim 37, wherein the channel signals are grouped into a bug signal (figure 4 of Hogeboom '998 disclose the encoding unit 400 grouping data and control information channel signals and transmitting the signals on a data bus; column 4, lines 48-53 of Hogeboom '998 disclose the encoding unit grouping control information and clock signal).

Regarding claim 39, Park '004, Hogeboom '998 and Heflin '554 disclose the method of claim 38, wherein the individual channel signals are selected from the bus signal independently by the second network unit (column 4, lines 55-62 and figure 4 of Hogeboom '998 disclose the decoding unit receiving both data channel and control information/clock channel, in which the decoding unit sends data to the data processing device 408, and extracts clock information and control information from a channel based on an signal encoding protocol; since the decoding unit knows the signal encoding protocol, it is implied that the decoding unit can select channel and decode data without any instruction from the encoding unit or the first network unit).

Regarding claim 40, Park '004, Hogeboom '998 and Heflin '554 disclose the method of claim 39, wherein decoding is performed in the second network unit by a mask function, where the received bus signal is not sampled (column 6, lines 18-20 of Heflin '554 disclose not passing pulses that are shorter than a threshold, i.e. the decoding unit of Hogeboom '998 does not receive the pulses) and

the selection is made by masking out the un-required pulses (i.e. the decoding unit of Hogeboom '998 only receives pulses that are longer than or equal to a threshold).

Regarding claim 41, Park '004 discloses a circuit for clock synchronization between a first network unit (figure 3 of Park '004) and a second network unit (it is implied that there is a second network unit, since clock synchronization is done between a plurality of network units), comprising:

a clock recovery unit (unit 22 in figure 3 of Park '004) having at least one reference clock signal provided in the first network unit (reference timing signals A and B are provided to the unit 22 in figure 3 of Park '004);

a bus provisioning unit (CPU 24 in figure 3 of Park '004) with an encoding unit (unit 23 in figure 3 of Park '004) arranged in the first network unit where the encoding unit is used for creating a channel signal (Fsys1 signal in figure 3 of Park '004) from the reference clock signal (column 4, lines 49-55 of Park '004 disclose generating a system clock Fsys1 using a reference clock).

However, Park '004 does not explicitly disclose created pulses having different pulse width and pulse distance; a bus signal being created from a plurality of channel signals and forwarded to a decoder unit in the second network unit, where the selection of an individual channel signal from the bus signal is performed independently by the second network unit.

Hogeboom '998 discloses created pulses having different pulse width (figure 3 of Hogeboom '998 discloses a pulse with a fixed falling edge and a plurality of rising edges

50, 50', 50" and 50"', in which each rising edge is in a different phase; the pulses comprising the fixed falling edge and each rising edge have different widths) and

pulse distance (column 4, lines 48-53 and figure 4 of Hogeboom '998 discloses a data bus channel 404 and a control information/clock bus channel 406; data signal and the clock signal generally have different amount of information contained within, therefore it is implied that the signals have different frequency, i.e. defined distances of the pulses are different for different signals);

a bus signal being created from a plurality of channel signals (column 4, lines 48-53 and figure 4 of Hogeboom '998 discloses a data bus channel 404 and a control information/clock bus channel 406) and

forwarded to a decoder unit in the second network unit (figure 4 of Hogeboom '998 discloses decoding unit 402 receiving clock, control information and data),

where the selection of an individual channel signal from the bus signal is performed independently by the second network unit (column 4, lines 55-62 and figure 4 of Hogeboom '998 disclose the decoding unit receiving both data channel and control information/clock channel, in which the decoding unit sends data to the data processing device 408, and extracts clock information and control information from a channel based on an signal encoding protocol; since the decoding unit knows the signal encoding protocol, it is implied that the decoding unit can select channel and decode data without any instruction from the encoding unit or the first network unit).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to create a bus signal and forward the bus signal to

a second network unit, since the modification, as suggested in column 2, lines 12-15 of Hogeboom '998, provides an efficient means of achieving both a synchronous clock and a control channel integrated in a single signal path used with a high-speed parallel data bus.

Furthermore, Park '004 and Hogeboom '998 do not explicitly disclose coordinating created pulses having pulse width and pulse distance for simultaneous collision free real-time transmission of the clock signals.

Heflin '554 discloses coordinating pulses having pulse width (column 6, lines 18-20 of Heflin '554 disclose a pulse width filter on a second network unit, i.e. decoder of Hogeboom '998 is on the second network unit) and

pulse distance (column 6, lines 27-29 of Heflin '554 disclose a pulse limiter that limits the duration of a pulse to one clock cycle of the local oscillator clock; if a pulse's width is greater than a clock cycle of the local oscillator clock, then the pulse would overlap with another pulse with respect to the clock cycle of the local oscillator clock; therefore the pulse limiter limits the distance between two pulses to 0 or greater with respect to the clock cycle of the local oscillator clock)

for simultaneous collision free (i.e. pulse limiter of Heflin '554 prevents two pulses from being overlapped with respect to the clock cycle of the local oscillator clock, therefore the pulses are collision free)

real-time transmission of the clock signals (column 10, lines 22-26 of Heflin '554 disclose that pulse limiter prevents a count sequence of counter/divider from being delayed, i.e. processed without delay or real-time).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a pulse width filter and a pulse distance filter, since the modification, as suggested in column 6, lines 20-22 of Heflin '554, prevents noise spikes from driving the synchronization circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOON J. CHUNG whose telephone number is (571)272-4059. The examiner can normally be reached on Monday - Thursday, 8:00AM - 5:00PM, ALT. Fridays, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Aung Moe can be reached on (571)272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aung S. Moe/
Supervisory Patent Examiner, Art Unit 2416

/Hoon J Chung/
Examiner, Art Unit 2416
May 05, 2009